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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/786,543	02/26/2004	Hiroshi Otani	249368US2	3261
22850	7590	10/06/2004	EXAMINER	
OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C. 1940 DUKE STREET ALEXANDRIA, VA 22314			QUINTO, KEVIN V	
			ART UNIT	PAPER NUMBER
			2826	

DATE MAILED: 10/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/786,543

Applicant(s)

OTANI, HIROSHI

Examiner

Kevin Quinto

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 26 February 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-9 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-9 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 112

1. Claims 1-9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.
2. Claim 1 contains the limitation "said potential drawing portion of said one semiconductor substrate is formed at a corner portion thereof and an area of said corner portion of said one semiconductor substrate including said potential drawing portion is almost equal to or less than an area of each of said potential drawing portions of said other semiconductor substrates." The examiner has found this limitation to be indefinite since the dimensions and area of the potential drawing portions are not clearly defined by the specification. Figure 3 of the applicant's specification is described as meeting this limitation (p. 8, lines 23-25 and p. 9, lines 1-3). However the specification fails to point out where each of the potential drawing portions begins and ends *since they are all each formed from a continuous piece of semiconductor material.*

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1 and 3 are rejected under 35 U.S.C. 102(b) as being anticipated by Yagi et al. (USPN 5,349,858).

5. So far as understood in claims 1 and 3, Yagi et al. (USPN 5,349,858, hereinafter referred to as the “Yagi” reference) discloses a similar device. Figure 11 of Yagi discloses a semiconductor device with an upper substrate (46) on which a plurality of through holes (56-59) are formed. There is a lower substrate (47). A plurality of semiconductor substrates (41, 42, 44) are provided between the upper substrate (46) and the lower substrate (47). The plurality of the semiconductor substrates (41, 42, 44) form a fixed electrode (41) and a variable electrode (42 or 44). Each of the electrodes have a potential drawing portion on an end portion which abuts the through holes (56-59) to draw potentials. One (41) of the plurality of the semiconductor substrates is formed to surround a periphery of the region between the upper substrate (46) and the lower substrate (47) like an outer frame. The other semiconductor substrates (42, 44) are surrounded by an inner periphery of the outer peripheral frame formed by one (41) of the semiconductor substrates. The potential drawing portion of the one semiconductor substrate (41) is formed at a corner portion and an area of the corner portion of the semiconductor substrate including the potential drawing portion is almost

equal to or less than an area of each of said potential drawing portions of said other semiconductor substrates.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yagi et al. (USPN 5,349,858) in view of Wolf and Tauber, ("Silicon Processing for the VLSI Era, Volume 2 – Process Integration," p. 851-852) and further in view of Schulte (USPN 4,391,032).

8. So far as understood in claim 2, there is a plurality of bonding pad portions (60-63) on a surface of the upper substrate (46). It is understood that these bonding pad portions serve to draw potentials from the potential drawing portions of the semiconductor substrates to the upper substrate through the through holes. Yagi does not disclose the use of bonding wires as a connective means but the use of bonding wires is well known in the art. Wolf and Tauber, ("Silicon Processing for the VLSI Era, Volume 2 – Process Integration," p. 851-852, hereinafter referred to as the "Wolf" reference) discloses the use of Au and Al wire bonding and states that it is a mature process. Schulte (USPN 4,391,032) states using a mature process is desired in the art since they lead to a technically simple and cost-saving process (column 4, lines 7-11).

In view of Wolf and Schulte, it would therefore be obvious to use wire bonding in the device of Yagi.

9. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yagi et al. (USPN 5,349,858) in view of Ristic et al. (USPN 5,545,912).

10. So far as understood in claim 4, Yagi does not disclose the use of a conductive layer on the surface of the upper substrate in order to shield the semiconductor substrates from a disturbance such as a proximity to other substances, static electricity, and radio waves. However the use of such a layer is well known in the art. Ristic et al. (USPN 5,545,912, hereinafter referred to as the "Ristic" reference) discloses the use of such a conductive layer in figure 1. Ristic discloses that this construct has the advantages of acting as an EMI shield, and providing protection against electrostatic discharge and adverse environments (column 5, lines 39-51) which are desirable in the art (column 1, lines 10-42). In view of Rustic, it would therefore be obvious to implement a conductive layer on the surface of the upper substrate in order to shield the semiconductor substrates from a disturbance such as a proximity to other substances, static electricity, and radio waves.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Quinto whose telephone number is (571) 272-1920. The examiner can normally be reached on M-F 8AM-5PM.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KVQ

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